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<u>L1</u>	(transaction or task or job) near3 reorder\$3	320	<u>L1</u>

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2	<input type="checkbox"/>	<input type="checkbox"/>	US 6785752 B2	20040831	18	Method for dynamically adjusting buffer utilization	710/56	710/60; 711/112
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6766388 B2	20040720	20	Method for determining a host data transfer goal in a	710/58	710/29; 710/60
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6721816 B1	20040413	12	Selecting independently of tag values a given command	710/6	710/240; 710/244;
5	<input type="checkbox"/>	<input type="checkbox"/>	US RE38428 E	20040210	37	Bus transaction reordering in a computer system having	710/110	370/402; 709/208;
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6622187 B1	20030916	12	Method for pre-processing data packets	710/100	710/305
7	<input type="checkbox"/>	<input type="checkbox"/>	US 5996036 A	19991130	36	Bus transaction reordering in a computer system having	710/110	709/208; 710/107
8	<input type="checkbox"/>	<input type="checkbox"/>	US 5930822 A	19990727	8	Method and system for maintaining strong ordering	711/150	711/158
9	<input type="checkbox"/>	<input type="checkbox"/>	US 5930485 A	19990727	50	Deadlock avoidance in a computer system having	710/112	710/110; 710/113;
10	<input type="checkbox"/>	<input type="checkbox"/>	US 5903738 A	19990511	19	Method and apparatus for performing bus transactions	710/105	710/112
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Jun Ma Parhi, K.K. Deprettere, E.F.
 Dept. of Electr. & Comput. Eng., Minnesota Univ., Minneapolis, MN, USA;
This paper appears in: Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on]

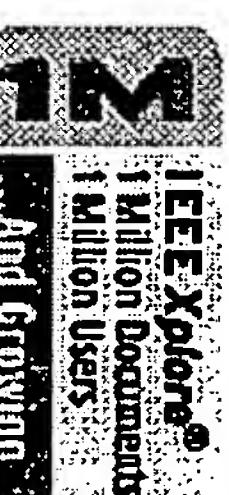
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Abstract:
 The novel annihilation-reordering look-ahead technique is proposed as an attractive technique for pipelining of Givens rotation (or CORDIC)-based adaptive filters. Unlike the existing relaxed look-ahead, the annihilation-reordering look-ahead does not depend on the statistical properties of the input samples. It is an exact look-ahead based on CORDIC arithmetic, which is known to be numerically stable. The conventional look-

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Annihilation-reordering look-ahead pipelined CORDIC-based RLS adaptive filters and their application to adaptive beamforming
Jun Ma [Parhi, K.K.](#) [Deprettere, E.F.](#)
Dept. of Electr. & Comput. Eng., Minnesota Univ., Minneapolis, MN, USA;
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Abstract:

The novel annihilation-reordering look-ahead technique is proposed as an attractive technique for pipelining of Givens rotation (or CORDIC)-based adaptive filters. Unlike the existing relaxed look-ahead, the annihilation-reordering look-ahead does not depend on the statistical properties of the input samples. It is an exact look-ahead based on CORDIC arithmetic, which is known to be numerically stable. The conventional look-

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ahead is based on multiply-add arithmetic. The annihilation-reordering look-ahead technique transforms an orthogonal sequential adaptive filtering algorithm into an equivalent orthogonal concurrent one by creating additional concurrency in the algorithm. Parallelism in the transformed algorithm is explored and different implementation styles including pipelining, block processing, and incremental block processing are presented. Their complexities are also studied and compared. The annihilation-reordering look-ahead is employed to develop fine-grain pipelined QR decomposition-based RLS adaptive filters. Both QRD-RLS and inverse QRD-RLS algorithms are considered. The proposed pipelined architectures can be operated at **arbitrarily** high sample rate without degrading the filter convergence behavior. Stability under finite-precision arithmetic are studied and proved for the proposed architectures. The pipelined CORDIC-based RLS adaptive filters are then employed to develop high-speed linear constraint minimum variance (LCMV) adaptive beamforming algorithms. Both QR decomposition-based minimum variance distortionless response (MVDR) realization and generalized sidelobe canceller (GSC) realization are presented. The complexity of the pipelined architectures are analyzed and compared. The proposed architectures can be operated at **arbitrarily** high sample rate and consist of only Givens rotations, which can be scheduled onto CORDIC arithmetic-based processors

Index Terms:

adaptive filters adaptive signal processing array signal processing computational complexity convergence of numerical methods digital filters least squares approximations parallel algorithms pipeline arithmetic recursive estimation CORDIC arithmetic CORDIC-based RLS adaptive filters Givens rotation LCMV adaptive beamforming algorithms QRD-RLS algorithm annihilation-reordering look-ahead pipelined filter block processing complexities exact look-ahead filter convergence fine-grain pipelined QR decomposition finite-precision arithmetic generalized sidelobe canceller high sample rate incremental block processing inverse QRD-RLS algorithm linear constraint minimum variance minimum variance distortionless response multiply-add arithmetic numerically stable look-ahead orthogonal concurrent filtering algorithm orthogonal sequential adaptive filtering algorithm pipelined architectures

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L5: Entry 1 of 12

File: USPT

Nov 16, 2004

US-PAT-NO: 6820151

DOCUMENT-IDENTIFIER: US 6820151 B2

TITLE: Starvation avoidance mechanism for an I/O node of a computer system

DATE-ISSUED: November 16, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ennis; Stephen C.	Austin	TX		

US-CL-CURRENT: 710/240; 710/309, 710/40, 710/5, 710/52, 710/53, 710/6

2. Document ID: US 6760792 B1

L5: Entry 2 of 12

File: USPT

Jul 6, 2004

US-PAT-NO: 6760792

DOCUMENT-IDENTIFIER: US 6760792 B1

TITLE: Buffer circuit for rotating outstanding transactions

3. Document ID: US 6760791 B1

L5: Entry 3 of 12

File: USPT

Jul 6, 2004

US-PAT-NO: 6760791

DOCUMENT-IDENTIFIER: US 6760791 B1

TITLE: Buffer circuit for a peripheral interface circuit in an I/O node of a computer system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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4. Document ID: US 6715055 B1

L5: Entry 4 of 12

File: USPT

Mar 30, 2004

US-PAT-NO: 6715055

DOCUMENT-IDENTIFIER: US 6715055 B1

TITLE: Apparatus and method for allocating buffer space

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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5. Document ID: US RE38428 E

L5: Entry 5 of 12

File: USPT

Feb 10, 2004

US-PAT-NO: RE38428

DOCUMENT-IDENTIFIER: US RE38428 E

TITLE: Bus transaction reordering in a computer system having unordered slaves

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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6. Document ID: US 6681274 B2

L5: Entry 6 of 12

File: USPT

Jan 20, 2004

US-PAT-NO: 6681274

DOCUMENT-IDENTIFIER: US 6681274 B2

TITLE: Virtual channel buffer bypass for an I/O node of a computer system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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7. Document ID: US 6163835 A

L5: Entry 7 of 12

File: USPT

Dec 19, 2000

US-PAT-NO: 6163835

DOCUMENT-IDENTIFIER: US 6163835 A

TITLE: Method and apparatus for transferring data over a processor interface bus

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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8. Document ID: US 5996036 A

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e e ef b e

L5: Entry 8 of 12

File: USPT

Nov 30, 1999

US-PAT-NO: 5996036

DOCUMENT-IDENTIFIER: US 5996036 A

TITLE: Bus transaction reordering in a computer system having unordered slaves[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequences](#) | [Attachments](#) | [Claims](#) | [KMC](#) | [Drawn De](#) 9. Document ID: US 5949981 A

L5: Entry 9 of 12

File: USPT

Sep 7, 1999

US-PAT-NO: 5949981

DOCUMENT-IDENTIFIER: US 5949981 A

TITLE: Deadlock avoidance in a bridge between a split transaction bus and a single envelope bus

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequences](#) | [Attachments](#) | [Claims](#) | [KMC](#) | [Drawn De](#) 10. Document ID: US 5933612 A

L5: Entry 10 of 12

File: USPT

Aug 3, 1999

US-PAT-NO: 5933612

DOCUMENT-IDENTIFIER: US 5933612 A

TITLE: Deadlock avoidance in a split-bus computer system

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequences](#) | [Attachments](#) | [Claims](#) | [KMC](#) | [Drawn De](#)[Clear](#)[Generate Collection](#)[Print](#)[Fwd Refs](#)[Bkwd Refs](#)[Generate OACS](#)

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Documents

L2 and L4

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L5: Entry 5 of 12

File: USPT

Feb 10, 2004

US-PAT-NO: RE38428

DOCUMENT-IDENTIFIER: US RE38428 E

TITLE: Bus transaction reordering in a computer system having unordered slaves

DATE-ISSUED: February 10, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kelly; James D.	Scotts Valley	CA		
Regal; Michael L.	Pleasanton	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 10/ 006939 [PALM]

DATE FILED: November 30, 2001

REISSUE-DATA:

US-PAT-NO	DATE-ISSUED	APPL-NO	DATE-FILED
05996036	November 30, 1999	779632	January 7, 1997

PARENT-CASE:

.Iadd.This application is a continuation-in-part of U.S. patent application Ser. No. 08/432,622, filed May 2, 1995, now abandoned..Iaddend.

INT-CL: [07] G06 F 9/46, G06 F 13/36, G11 C 7/00

US-CL-ISSUED: 710/110; 710/107, 709/208, 370/402

US-CL-CURRENT: 710/110; 370/402, 709/208, 710/107

FIELD-OF-SEARCH: 710/110, 710/107, 710/263, 710/41, 710/52, 710/311, 709/100, 709/208, 714/47, 711/151, 370/402

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <u>4181974</u>	January 1980	Lemay et al.	

<input type="checkbox"/>	<u>4473880</u>	September 1984	Budde et al.
<input type="checkbox"/>	<u>4494193</u>	January 1985	Brahm et al.
<input type="checkbox"/>	<u>4965716</u>	October 1990	Sweeney
<input type="checkbox"/>	<u>5006982</u>	April 1991	Ebersole et al.
<input type="checkbox"/>	<u>5191649</u>	March 1993	Cadambi et al.
<input type="checkbox"/>	<u>5257356</u>	October 1993	Brockmann et al.
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<input type="checkbox"/>	<u>5327538</u>	July 1994	Hamaguchi et al.
<input type="checkbox"/>	<u>5327570</u>	July 1994	Foster et al.
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<input type="checkbox"/>	<u>5345562</u>	September 1994	Chen
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<input type="checkbox"/>	<u>5418914</u>	May 1995	Heil et al.
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<input type="checkbox"/>	<u>5473762</u>	December 1995	Krein et al.
<input type="checkbox"/>	<u>5542056</u>	July 1996	Jaffa et al.
<input type="checkbox"/>	<u>5544332</u>	August 1996	Chen
<input type="checkbox"/>	<u>5546546</u>	August 1996	Bell et al.
<input type="checkbox"/>	<u>5592631</u>	January 1997	Kelly et al.
<input type="checkbox"/>	<u>5592670</u>	January 1997	Pletcher
<input type="checkbox"/>	<u>5615343</u>	March 1997	Sarangdhar et al.
<input type="checkbox"/>	<u>5680402</u>	October 1997	Olnowich et al.
<input type="checkbox"/>	<u>5682512</u>	October 1997	Tetrick
<input type="checkbox"/>	<u>5708794</u>	January 1998	Parks et al.
<input type="checkbox"/>	<u>5822772</u>	October 1998	Chan et al.
<input type="checkbox"/>	<u>5930485</u>	July 1999	Kelly
<input type="checkbox"/>	<u>5933612</u>	August 1999	Kelly et al.

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

h e b b cg b cc e

ATTY-AGENT-FIRM: Fenwick & West LLP

ABSTRACT:

A mechanism is provided for reordering bus transactions to increase bus utilization in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, both masters and slaves are ordered, simplifying implementation. In another embodiment, the system is more loosely coupled with only masters being ordered. Greater bus utilization is thereby achieved. To avoid deadlock, transactions begun on the split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. In the more tightly coupled system, the predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In the more loosely-coupled system, the flexibility afforded by unordered slaves is taken advantage of to, in the typical case, reorder the transactions and avoid deadlock without killing any transaction. Where a data dependency exists that would prevent such reordering, the further transactions is killed as in the more tightly-coupled embodiment. Data dependencies are detected in accordance with address-coincidence signals generated by slave devices on a cache-line basis. In accordance with a further optimization, at least one slave device (e.g., DRAM) generates page-coincidence bits. When two transactions to the slave device are to the same address page, the transactions are reordered if necessary to ensure that they are executed one after another without any intervening transaction. Latency of the slave is thereby reduced.

19 Claims, 27 Drawing figures

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L5: Entry 8 of 12

File: USPT

Nov 30, 1999

US-PAT-NO: 5996036

DOCUMENT-IDENTIFIER: US 5996036 A

TITLE: Bus transaction reordering in a computer system having unordered slaves

DATE-ISSUED: November 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kelly; James D.	Aptos	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computers, Inc.	Cupertino	CA			02

APPL-NO: 08/ 779632 [PALM]

DATE FILED: January 7, 1997

INT-CL: [06] G06 F 9/46, G06 F 13/36, G11 C 7/00

US-CL-ISSUED: 710/110; 710/107, 709/208

US-CL-CURRENT: 710/110; 709/208, 710/107

FIELD-OF-SEARCH: 710/110, 710/107, 710/263, 710/41, 710/52, 711/151, 709/100-102, 709/208

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

 [Search Selected](#) [Search All](#) [Clear](#)

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <u>4181974</u>	January 1980	Lemay et al.	364/900
<input type="checkbox"/> <u>4473880</u>	September 1984	Budde et al.	364/200
<input type="checkbox"/> <u>4965716</u>	October 1990	Sweeney	364/200
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<input type="checkbox"/> <u>5191649</u>	March 1993	Cadambi et al.	395/200
<input type="checkbox"/> <u>5257356</u>	October 1993	Brockmann et al.	395/725
<input type="checkbox"/> <u>5287477</u>	February 1994	Johnson et al.	395/425
<input type="checkbox"/> <u>5327538</u>	July 1994	Hamaguchi et al.	395/325

<input type="checkbox"/>	<u>5345562</u>	September 1994	Chen	395/275
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<input type="checkbox"/>	<u>5473762</u>	December 1995	Krein et al.	395/287
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<input type="checkbox"/>	<u>5682512</u>	October 1997	Tetrick	711/202
<input type="checkbox"/>	<u>5822772</u>	October 1998	Chan et al.	711/158

ART-UNIT: 271

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, L.L.P.

ABSTRACT:

A mechanism is provided for reordering bus transactions to increase bus utilization in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, both masters and slaves are ordered, simplifying implementation. In another embodiment, the system is more loosely coupled with only masters being ordered. Greater bus utilization is thereby achieved. To avoid deadlock, transactions begun on the split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. In the more tightly coupled system, the predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In the more loosely-coupled system, the flexibility afforded by unordered slaves is taken advantage of to, in the typical case, reorder the transactions and avoid deadlock without killing any transaction. Where a data dependency exists that would prevent such reordering, the further transactions is killed as in the more tightly-coupled embodiment. Data dependencies are detected in accordance with address-coincidence signals generated by slave devices on a cache-line basis. In accordance with a further optimization, at least one slave device (e.g., DRAM) generates page-coincidence bits. When two transactions to the slave device are to the same address page, the transactions are reordered if necessary to ensure that they are executed one after another without any intervening transaction. Latency of the slave is thereby reduced.

17 Claims, 26 Drawing figures

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L5: Entry 9 of 12

File: USPT

Sep 7, 1999

US-PAT-NO: 5949981

DOCUMENT-IDENTIFIER: US 5949981 A

TITLE: Deadlock avoidance in a bridge between a split transaction bus and a single envelope bus

DATE-ISSUED: September 7, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Childers; Brian Alan	Santa Clara	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 888113 [\[PALM\]](#)

DATE FILED: July 3, 1997

PARENT-CASE:

This application is a continuation of application Ser. No. 08/432,621, filed May 2, 1995, now abandoned.

INT-CL: [06] [G06 F 13/00](#)

US-CL-ISSUED: 395/309; 395/308, 395/287

US-CL-CURRENT: [710/310](#); [710/107](#)

FIELD-OF-SEARCH: 395/306-309, 395/287

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> 4494193	January 1985	Brahm et al.	395/200.06
<input type="checkbox"/> 5278974	January 1994	Lemmon et al.	395/550
<input type="checkbox"/> 5305442	April 1994	Pedersen et al.	395/290
<input type="checkbox"/> 5345562	September 1994	Chen	395/275
<input type="checkbox"/> 5355455	October 1994	Hilgendorf et al.	395/306

<input type="checkbox"/>	<u>5363485</u>	November 1994	Nguyen et al.	395/250
<input type="checkbox"/>	<u>5418914</u>	May 1995	Heil et al.	395/293
<input type="checkbox"/>	<u>5469435</u>	November 1995	Krein et al.	370/85.2
<input type="checkbox"/>	<u>5546546</u>	August 1996	Bell et al.	395/292

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
9532475	November 1995	WO	

ART-UNIT: 271

PRIMARY-EXAMINER: An; Meng-Ai T.

ASSISTANT-EXAMINER: Lefkowitz; Sumati

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, L.L.P.

ABSTRACT:

A mechanism is provided for avoiding deadlock, in particular, a Read/Read deadlock, in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, deadlock is avoided using a closely-coupled master and slave circuit on the split-response bus. The closely-coupled master and slave circuit operates to disallow a second deadlocking read transaction. While there is an outstanding read transaction in either the master or slave portions of the split-response bus interface, the other portion will refuse to accept, or retry, another potentially deadlocking read transaction. The invention has the advantage of being absolutely certain of avoiding the Read/Read deadlock condition with a minimum amount of circuit complexity.

8 Claims, 7 Drawing figures

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United States Patent [19]

Kelly

[11] Patent Number: 5,930,485

[45] Date of Patent: Jul. 27, 1999

[54] DEADLOCK AVOIDANCE IN A COMPUTER SYSTEM HAVING UNORDERED SLAVES

[75] Inventor: James D. Kelly, Aptos, Calif.

[73] Assignee: Apple Computer, Inc., Cupertino, Calif.

[21] Appl. No.: 08/779,913

[22] Filed: Jan. 7, 1997

Related U.S. Application Data

[51] Int. Cl. 6 G06F 13/14; G06F 13/40

[52] U.S. Cl. 395/292; 395/290; 395/293;

395/308

[58] Field of Search 395/290, 292, 395/293, 308, 309, 728, 729

[56] References Cited

U.S. PATENT DOCUMENTS

4,494,193	1/1985	Brahm et al.	364/200
5,305,442	4/1994	Pedersen et al.	395/325
5,355,453	10/1994	Hilgeodorf et al.	395/325
5,363,485	11/1994	Nguyen et al.	395/250
5,418,914	5/1995	Heil et al.	395/325
5,442,763	8/1995	Bartfai et al.	395/375
5,469,435	11/1995	Krein et al.	370/85.2
5,473,762	12/1995	Krein et al.	395/287
5,542,056	7/1996	Jaffa et al.	395/306
5,544,332	8/1996	Chen	395/288
5,546,546	8/1996	Bell et al.	395/292
5,592,631	1/1997	Kelly et al.	395/293
5,592,670	1/1997	Pletcher	395/670
5,615,343	3/1997	Sarangdhar et al.	395/282
5,680,402	10/1997	Olinowich et al.	370/498
5,708,794	1/1998	Parks et al.	395/481

Primary Examiner—Ayaz R. Sheikh

Assistant Examiner—Nigar Pancholi

Attorney, Agent, or Firm—Burns, Doane, Swecker & Mathis, LLP

[57] ABSTRACT

A mechanism is provided for reordering bus transactions to increase bus utilization in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, both masters and slaves are ordered, simplifying implementation. In another embodiment, the system is more loosely coupled with only masters being ordered. Greater bus utilization is thereby achieved. To avoid deadlock, transactions begun on said split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. In the more tightly coupled system, the predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In the more loosely-coupled system, the flexibility afforded by unordered slaves is taken advantage of to, in the typical case, reorder the transactions and avoid deadlock without killing any transaction. Where a data dependency exists that would prevent such reordering, the further transaction is killed as in the more tightly-coupled embodiment. Data dependencies are detected in accordance with address-coincidence signals generated by slave devices on a cache-line basis. In accordance with a further optimization, at least one slave device (e.g., DRAM) generates page-coincidence bits. When two transactions to the slave device are to the same address page, the transactions are reordered if necessary to ensure that they are executed one after another without any intervening transaction. Latency of the slave is thereby reduced.

24 Claims, 21 Drawing Sheets

